

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:)	
)	
Wang-Jin Chen)	Confirmation No.: 9153
)	
Serial No.: 10/733,095)	Group Art Unit: 2825
)	
Filed: December 11, 2003)	Examiner: Rossoshek, Yelena
)	
For: I/O CIRCUIT PLACEMENT METHOD AND)	TKHR Ref. 250606-1020
SEMICONDUCTIVE DEVICE)	Top-Team ref. 0697-10333US
)	
)	
)	

AMENDMENT AND RESPONSE TO FINAL OFFICE ACTION

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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

The FINAL Office Action mailed, May 16, 2006 has been carefully considered. In response thereto, Applicant respectfully requests consideration of the following remarks.

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (currently amended) An I/O circuit placement method for placing I/O circuits included in a semiconductor device, comprising a step of:

placing at least two rows of I/O circuits on a first side of a chip, wherein each I/O circuit has a head section and a tail section, the head section and the tail section are arranged in a column direction perpendicular to a row direction of the I/O circuits, wherein the head sections of at least one of the two rows are oriented to the tail sections in the adjacent rows, the tail section transfer signals to and from external devices and the head section serves as an interface circuit between the tail section and a core circuit region to convert signal level.

2. (original) The placement method as claimed in claim 1 further comprises a step of placing another row of I/O circuits on a second side of the chip.

3~4. (cancelled).

5. (original) The placement method as claimed in claim 1, wherein a different number of I/O circuits are placed in different rows.

6. (currently amended) A semiconductor device, comprising:

a chip; and

at least two rows of I/O circuits placed on a first side of the chip, wherein each I/O circuit has a head section and a tail section, the head section and the tail section are arranged in a column direction perpendicular to a row direction of the I/O circuits, wherein the head sections of at least one of the two rows are oriented to the tail sections in the adjacent rows, the tail section transfer signals to and from external devices and the head section serves as an interface circuit between the tail section and a core circuit region to convert signal level.

7. (original) The semiconductor device as claimed in claim 6, further comprising another row of I/O circuits placed on a second side of the chip.

8~10. (cancelled)

11. (previously amended) The semiconductor device as claimed in claim 6, wherein the core circuit region is disposed on the chip, and the rows of I/O circuits are disposed outside the core circuit region and are at the periphery of the chip.

12. (original) The semiconductor device as claimed in claim 6, wherein the number of the I/O circuits placed in the different rows is different.

13. (currently amended) A semiconductor device, comprising:

a chip;

a core circuit region disposed on the chip;

a loop of I/O circuits disposed at the periphery of the chip and around the core circuit

region; and

at least one row of I/O circuits disposed between the loop of I/O circuits and the core

circuit region, wherein each I/O circuit has a head section and a tail section, and

the head sections of the row are oriented to the tail sections in an adjacent row.

14~16. (cancelled).

REMARKS

The Examiner is thanked for the thorough examination of the present application and the indication that claims 3, 5, 8, 10, 12, 14, and 16 contain allowable subject matter. The Office Action, however, continued to reject the remaining claims. In response, independent claims 1, 6, and 13 have been amended. Claims 3-4, 8-10, and 14-16 have been canceled. After entry of the foregoing amendments, claims 1-2, 5-7, and 11-13 remain pending in this application, and reconsideration of these claims is respectfully requested.

Response To Objection of Claim 13

The Office Action objected to claim 13 for certain informalities. In response, claim 13 has been amended to particularly point out and distinctly claim the subject matter of the present invention for overcome this objection. Specifically, claim 13 is amended to specify that the at least one row of I/O circuits is disposed between the loop of I/O circuits and the core circuit region. As described on lines 11-21 in page 2 of the specification, the rows 20, 21, 26, and 27 form a loop, and the rows (22~25 and 28) of I/O circuits are disposed between the loop of I/O circuits and the core circuit region. Accordingly, support for the amended language can be found in at least Fig. 2 and the specification of the present application. No new matter has been added.

Response To Claim Rejections Under 35 U.S.C. §102

Claims 1-2, 4, 6, 7, 9, 11, 13 and stand rejected under 35 U.S.C. §102(e) as allegedly anticipated by Iwasa (U.S. Patent No. 6721933). While Applicant disagrees with the rejection, in the interest of forwarding this application to early issuance, Applicant has amended

independent claims 1, 6, and 13 to include the allowable subject matter of other claims.

Specifically, in reliance on the indicated allowable subject matter, independent claims 1, 6, and 13 have been amended to include the respective limitations of dependent claims 3, 8, and 14.

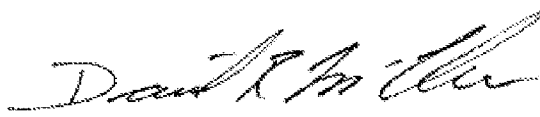
Therefore, claims 1, 6, and 13 as amended are clearly allowable, based on the admissions of the Office Action. All remaining claims depend from claims 1, 6, or 13, and therefore patently define over the prior art for at least the same reasons.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to FINAL Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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